REMARKS

I. Status of the Claims

Claims 1 - 8 have been examined and stand rejected on various grounds.

II. Objections to the Claims

The Office Action identified insufficient antecedent bases for various limitations in claims 2 - 4, due to a lack of a dependency phrase in each of the claims. These claims have been amended for the sole purpose of adding the dependency on claim 1.

III. Rejections Under 35 U.S.C. §102

The Examiner rejected claims 1, 2 and 8 as being anticipated by U.S. Patent 5,426,563 to Moresco, et al. According to the Examiner, Moresco describes all of the claimed features recited in claims 1, 2 and 8. The Applicant respectfully disagrees.

A) Claim 1

Claim 1 is directed to a printed circuit board assembly that minimizes parts and weight to enable immersion cooling of semiconductor devices mounted on the boards. Those devices may include individual integrated circuits, or somewhat larger multi-chip modules, which house a plurality of ICs in a single package. The PCB assembly of claim 1 places a pair of boards with the device sides in confronting parallel relationship (the devices of both boards face each other). A border is formed at the periphery between the boards to form a liquid seal. An inlet and outlet are also provided to allow for a non-conductive coolant to enter and exit the assembly.

Moresco describes an internal construction for a multi-chip module. Again, a multi-chip module is packaged much like a single integrated circuit, yet includes a larger package to house multiple IC's. Multi-chip module constructions such as that disclosed in Moresco have nothing to do with printed circuit board assemblies, as that term is commonly understood in the art.

Nevertheless, Moresco's multi-chip module includes, within its package, a plurality of tiny stacked substrates, each substrate mounting a plurality of semiconductor devices in the same orientation. In other words, the bottom of one substrate is stacked

over the top of another substrate. The substrates are spaced apart by bars 150, which also define walls defining coolant paths, or coolant channels. A package is placed around the entire stacked assembly and interconnects are formed to connect the package to a circuit board or other electronic assembly.

It is well known that anticipation under 35 U.S.C. §102 requires that each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. In re Robertson, 169 F.3d 743, 49 U.S.P.Q.2d 1949 (Fed. Cir. 1999)(*reversing Board of Patent Appeals & Interference's finding of anticipation under §102*).

Contrary to the rationale offered in the Office Action, Moresco fails to disclose or remotely suggest many of the structural features of claim 1. First of all, Moresco describes a device (multi-chip module) for mounting to a circuit board. His internal module construction is not a printed circuit board assembly as claimed in claim 1.

Further, claim 1 recites that the printed circuit boards have device sides disposed in **confronting** relationship. This means that the device sides of each board face each other. This eliminates the need for an additional "lid" to seal the top of the assembly. Instead, a border is provided around the periphery of the boards to provide a liquid seal. Not only does Moresco fail to configure his substrates in confronting relationship, but the disclosure also explains the need for an additional lid in column 8, lines 45 - 50.

For all of the above reasons, claim 1 is believed allowable over the cited art and reconsideration is requested. Because claims 3 and 4 depend from claim 1, these claims are also believed allowable.

B) Claim 2

Claim 2 recites that the first and second circuit boards of claim 1 comprise channel cards for use in a semiconductor tester.

With all due respect to the Examiner, while Moresco has the word "channel" in column 8, lines 51 - 54, the disclosure relates to openings or paths for fluid (coolant) flow. This has nothing to do with electronic channels for routing electrical signals. Moresco also has no relevance to semiconductor testers. For these reasons, claim 2 is believed allowable over the cited art and reconsideration is respectfully requested.

C) Claim 8

As noted above with respect to claim 1, Moresco fails to mount devices on **confronting** sides of parallel substrates. His construction also fails to interpose a border between the substrates. For these reasons claim 8 is allowable over the cited art.

IV. Rejections Under 35 U.S.C. §103

The Office Action identified rejections to claims 3, 4, 5, 6 and 7 under 35 U.S.C. 103 as being unpatentable over Moresco et al in view of Black (U.S. Patent No. 4,749,943).

According to the Examiner, Black discloses that it is well-known in the art to test printed circuit boards with a computer workstation and a testhead adapted for being carried by a manipulator.

Claim 5 relates to the construction of circuit board assemblies employed in automatic test equipment. These are relatively large assemblies that include up to several hundred packaged devices mounted on an individual board. Consequently the boards may weigh twenty to fifty pounds, or more. Moresco, on the other hand, relates to the internal construction of a single packaged device, weighing, perhaps, a few ounces.

Black discloses a printed circuit board tester, a form of automatic test equipment. However, Black reveals no teachings on cooling the boards that are used inside the tester.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

It is unclear what, if any, motivation exists to combine the Moresco and Black references. However, even if they were combined, they do not disclose all of the claimed features of claim 5.

As to claims 4 and 7, Moresco teaches mounting all of his devices on the same side of each substrate. Claims 4 and 7, however, recite devices mounted on opposed, or confronting sides. This eliminates the need for a lid, such as that required for Moresco.

Claims 3 and 6 relate to the seal construction for the border feature of claims 1

and 5. Because the border has top and bottom sealing edges, respective first and second seals are employed. Suga, on the other hand, describes a lid assembly (most likely similar to the lid recommended by Moresco) that includes one seal for disposition between the marginal edge of the lid and the board being sealed. Suga does not describe first and second seals as claimed in claims 3 and 6. Reconsideration is requested.

For all of the above reasons, claims 3, 4, 5, 6 and 7 are believed allowable over the cited art.

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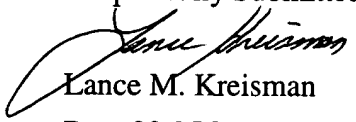
Respectfully Submitted



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